ATTACHMENT A

Remarks

Considering the matters raised in the Office Action in the same order as raised, the disclosure has been objected to because of certain informalities. The suggestions of the Examiner with respect to these informalities have been adopted. The Examiner is thanked for the assistance provided in this regard.

Claims 1-18 have been objected to because of certain informalities. The claims have been amended to address these informalities and, in particular, all of the suggestions of the Examiner have been adopted in amending the claims. Again, the assistance of the Examiner is appreciated.

Claims 3-6 and 12-15 have been rejected under 35 U.S.C. 112, first paragraph, as "failing to comply with the enablement requirement." This rejection is respectfully traversed.

It is alleged in the Office Action that the claims contain "subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or which it is most nearly connected, to make and/or use the invention." In particular, it is contended that the "claimed subject matter of claims 3-6 and 12-15 does not correspond to the disclosure of Figures 4b to 4e which was not described in a specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention." Further, it is contended that "[s]pecifically, the specification fails to describe the values 1 and 0 used in the logic gate(s) of Figures 4b to 4e to enable one skilled in the art to understand [the] invention."

Considering claims 3 to 6 as exemplary, these claims cover four different embodiments of the logic processing step (step c)) of claim 2. Claim 3 covers an embodiment wherein a first logic value of the envelope logic signal corresponds to the start and the end of a packet and is equal to a value zero (0) and a second logic value of the envelope logic signal is equal to the value one (1), wherein the logic processing step comprises applying to each received signal, an AND logic function with the

envelope logic signal. This can be represented as set forth below (wherein ELS indicates envelope logic signal).

first ELS = 0

AND ELS

second ELS = 1

Claim 4 is directed to a second embodiment corresponding to the start and end of a packet and equal to the value one (1) and with the envelope logic signal equal to the value zero (0), wherein the logic processing comprises applying to each received signal an OR logic function with the complemented envelope logic signal. This can be represented as set forth below.

first ELS = 1

OR $\overline{ELS}$

second ELS = 0

Claim 5 covers an embodiment with reverse logic values for the first and second logic values as in claim 3, using the same logic operator applied to the complemented envelope logic signal and can be represented as follows:

first ELS = 0

AND $\overline{ELS}$

second ELS = 1

Finally, claim 6 covers an embodiment with reverse logic values for the first and second logic values as in claim 4 using the same logic operator applied to the envelope logic signal, and can be represented as follows:

first ELS = 1

OR ELS

second ELS = 0

It is respectively submitted that the corresponding mode of operation is fully disclosed in the specification in, inter alia, paragraphs [0073] to [0078] and paragraphs [0085] to [0089], the latter of which describe Figures 4a to 4e, as pointed out by the Examiner. As shown in Figure 4a, the envelope logic signal E_j is ANDed, as claimed in claim 3, and as shown in Figure 4e, is ORed as claimed in claim 6, while the complemented value E_j is ORed as shown in Figure 4c and ANDed as shown in Figure 4d, as claimed in claims 4 and 5, respectively. Further, page 11, at lines 4 to 7, a non-restrictive example is described which comprises adding by concatenation at the start and at the end of the data packet P_j, "n" stable values 0 or 1. It is respectively submitted that concatenating stable values, viz., a 0 or 1 value, at the beginning and end of a data packet would be fully understood by one of ordinary skill in the art, and that the logic operations claimed are clearly disclosed in Figures 4a to 4e. Similar remarks apply, of course, to claims 12-15 which basically correspond to or track claims 3-6. Accordingly, withdrawal of the rejection of claims 3-6 and 12-15 is respectfully requested.

Claims 7-9 and 16-18 have been rejected under 35 U.S.C. 112, second paragraph, as being "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." In order to overcome this rejection, the phrase "said current packet" has been changed to read -- said packet -- so that a clear antecedent basis is provided.

Applicant gratefully acknowledges the indication that claims 1, 2, 7-11, and 16-18 would be "allowable if rewritten or amended to overcome the objection(s) set forth in this Office action" and that claims 7-9 and 16-18 would be "allowable if rewritten or amended to overcome the objection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action." Because these claims have been amended to overcome both the objections and rejections raised, it is respectively submitted that these claims are now in condition for allowance. Further, it is respectively submitted that dependent claims 3-6 and 12-15 should also be allowed along with the claims parent thereto, for the reasons set forth above.

Favorable action is respectively requested.

END REMARKS